SPI Technical Specification (public)

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Role

BX310x supports SPI slave role.

Hardware interface

The hardware interface uses five wires plus the ground connection.

Interface	Description	Note	GPIO number
MISO	Master In Slave Out	Data transfer from Slave to Master	13
MOSI	Master Out Slave In	Data transfer from Master to Slave	12
SCLK	Serial Clock	Data clock generated by Master	14
CS	Chip Select	Master ready to transfer data. Active low.	15
SRDY	Slave Ready	Slave ready to transfer data. Active high.	16

SPI Options

- Mode - Clock Polarity (CPOL) and Clock Phase (CPHA)
  - Configurable with AT+SRSPI command
  - Values:
    - 0: (Default) CPOL 0, CPHA 0
    - 1: CPOL 0, CPHA 1
    - 2: CPOL 1, CPHA 0
    - 3: CPOL 1, CPHA 1
  - Default: 0 - CPOL 0, CPHA 0
- Bit numbering
  - Configurable with AT+SRSPI command
  - Values:
    - 0: (Default) Transmit and receive MSB first.
    - 1: Transmit LSB first, receive MSB first.
    - 2: Transmit MSB first, receive LSB first.
    - 3: Transmit and receive LSB first.
  - Default value: 0 - Transmit and receive MSB first.
- Clock speed
  - Tested at 3 MHz

Protocol format

SPI Frame:

command	payload_length	more	reserved	payload
2 bytes	2 bytes	1 byte	3 bytes	256 bytes

- <command>:
  - 0x0001: AT command
  - 0x0002: AT response
  - 0x0003: data (data mode)
  - 0xffff: dummy data
- <payload_length>:
  - Length of the significant content in the payload
  - Range: 0-256
- <more>:
  - For command=0x0002, if more=1 it indicates that the AT response is not complete and that another frame will be sent after this one
- <payload>:
  - Payload is always 256 bytes long. The significant data could be less, <payload_length> indicate the length of the significant part of payload.
  - When sending a frame, the slave add 0 padding to the payload if necessary.
  - When receiving a frame, the slave will only process the data if <payload_length> and <payload> are coherent. Non significant part of <payload> is expected to be set to 0.

SPI "AT commands" differences from UART

- To exit data mode, a frame with only the escape sequence must be sent to the slave. If the escape sequence is included in a data frame sent to the slave, it will not be detected.
- When using AT+RST, the OK response may not be sent to the master (because the device is rebooting immediately afterwards, so there is not enough time for the response to be processed).

Hardware interface selection (UART/SPI)

If GPIO 17 is high when the module boots up, SPI will be selected, otherwise UART will be selected.

No labels